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09/360,025	07/23/1999	SHINKEN OKAMOTO	2418.05-US-0	3581

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EXAMINER	
AMANZE, EMEKA J	
ART UNIT	PAPER NUMBER
2133	

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Please find below and/or attached an Office communication concerning this application or proceeding.

KT

Office Action Summary	Application No. 09/360,025	Applicant(s) OKAMOTO, SHINKEN
	Examiner Emeka J. Amanze, JD	Art Unit 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 July 1999* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Reassignment Affecting Application

0. The Art Unit of your application in the USPTO has changed. To aid in correlating any papers for this application, all future correspondence regarding this application should be directed to Art Unit 2133.

DETAILED ACTION

Procedural History

1. Claims 1-12 are presented for examination.

Claim Relationships

2. Claims 1-5 are directed *to "a memory unit having a memory, a :memory status indicator and a processor, wherein the processor monitors the status of the memory and communicates memory status information to the memory status indicator"* Claims 6-12 are directed to *"a method of determining and indicating memory status, comprising the steps of: calculating a value representative of memory usage; comparing the calculated number with a pre-determined number; and changing a memory status indicator when the calculated number reaches the pre-determined number."*

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraph of 35 U.S.C. § 102 that forms the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3.1 Claims 1-12 are rejected under 35 U.S.C. § 102(e) as being fully anticipated by Yamagami *et al.* (US Patent No. 6,130,837 Jan. 1997).

As per claims 1 and 6:

Claims 1 and 6 are similar, except as noted above. *See, supra,* section 2. Claims 1 and 6 are rejected based on the following rationale.

As depicted in fig. 10, Yamagami *et al.* teach a memory unit employing flash memory (item 21) in which the file data are stored, and wherein an access controller (memory controller) (item 22) generates access signals which are directed to the flash memory, and wherein a processor (item 23) deals with stored data and status data, and constructs an external storage system based on the flash memory, and wherein a program memory (item 24) stores therein control programs for operating the processor. *See* col. 13, lines 58-67 (et seq.). Yamagami *et al.* also teaches the claimed invention wherein, a logical sector table (logical sector reference means, item 25) is for referring to the location of the flash memory at which the data of a sector (logical sector) indicated by a certain logical address (logical sector identification information) is mapped, while a physical sector table (physical sector reference means, item 26) is for referring to the logical sector No. of the file data which is mapped at a physical sector indicated by the physical address (physical sector identification information) of the flash memory 21. A number of erasures management table (number of erasures reference means, item 27) registers the cumulative numbers of erasures of a respective physical addresses, and a status table (status

reference means, item 28) is for referring to the statuses of the respective physical sectors, and wherein a write buffer (item 29) serves to temporarily store data to-be-written therein, for the purpose of quickening the operation of writing the data, so that the processor runs the programs stored in the program memory. *See id.*

Additionally, as depicted in fig. 2, Yamagami *et al.* teach the claimed method for indicating memory status including a memory map including an (error information area, item 71), a (usage information area, item 72), and a (substitutive memory area, item 73) wherein the said areas need to be separated in agreement with the boundaries of data writing blocks, such that the error information area is the area in which the error information corresponding to the individual blocks of the data memory (item 8) are stored, and wherein when the block is normal, the error information is denoted by FFFFh, and when the block is abnormal, the error information indicates the number of the block of the substitutive memory area substituting for the abnormal block, and the usage information area is the area which expresses the usage situation of the substitutive memory area, and in which usage information corresponding to the individual substitutive blocks of the substitutive memory area are stored, such one bit is allotted to each of the substitutive blocks, and when the corresponding substitutive block is used or occupied as the substitute, the usage information is denoted by "1", and when not, the usage information is denoted by "0". The unused or unoccupied block of the substitutive memory area can be found by seeking the bit of "0" in the usage information area , and the substitutive memory area is the area which substitutes for the error blocks of the data memory. *See* col. 4, lines 61-67 (et seq.). The respective blocks are endowed with the Nos. of the substitutive blocks successively from an address 20000h. *Id* at col. 4, lines 18-20.

As per claim 2:

As depicted in fig. 2, Yamagami *et al.* teach a means for the external display or indicator light, including a status reference means (item 28) (substitute "indicator") for referring to the statuses of the respective physical sectors. *See* col. 14, lines 15-23. In fig. 25, Tamagami *et al* depict an externally mounted buffer (item 29), which serves to temporarily store data to-be-written therein, for the purpose of quickening the operation of writing the data. *See also* col. 1, lines 33-44.

As per claim 3, 7, and 10:

Claims 3, 7, and 10 are similar, except as noted above. *See, supra,* section 2. Claims 3, 7, and 10 are rejected based on the following rationale.

Yamagami teach the claimed memory unit and method wherein a processor monitors write operations in memory. *See* col. 16, lines 6-16. As depicted in fig. 10, Yamagami *et al.* teach the claimed processor (item 23) mounted with fine controls that can be performed in accordance with the contents of the program memory (item 24). *Id.*

Additionally, Yamagami et al teach the claimed method for calculating memory usage wherein write error develops in the flash memory in a case where the limit of the number of rewrite operations of this flash memory has been exceeded due to the frequent write operations of only a specified block, and wherein the normal write operation is decided at the checking step. *See* col. 6, lines 35-44.

As per claims 4 and 11:

Claims 4 and 11 are similar, except as noted above. *See, supra,* section 2. Claims 4 and 11 are rejected based on the following rationale.

Yamagami et al. teach the claimed memory unit and method wherein the storage capacity of the substitutive memory areas may be afforded by predetermined ones of the data memory areas. *See* col. 13, lines 13-19. See also col. 9, lines 50-59, wherein Yamagami teaches a a substitutive memory area in correspondence with the number of blocks.of the data memory requiring a predetermined memory capacity of at least 80KB. .

As per claims 5 and 9:

Claims 5 and 9 are similar, except as noted above. *See, supra,* section 2. Claims 5 and 9 are rejected based on the following rationale.

Yamagami et al. teach the claimed memory unit and method wherein error memory areas may retain the error information of the substitutive memory areas having undergone errors, such that it possible to remedy, not only the errors of the data memory areas, but also the errors which have developed in the substitutive memory areas having once substituted for the data memory areas, and wherein the substitutive memory areas having undergone the errors may be replaced in the same manner as in the case where the errors have developed in the data memory areas. *See* col. 13, lines 1-11.

As per claims 8 and 12:

Claims 8 and 12 are similar. Claims 8 and 12 are rejected based on the following rationale.

As depicted in fig. 25, Yamagami *et al.* teach the claimed method wherein a first transfer means writes data to-be-written into the buffer area (item 142), and when an address is input, the second transfer means transfers a plurality of items of data to the corresponding data area (item 141) at one stroke so as to be written thereinto; and wherein in a read operation, a plurality of items of data can be transferred contrariwise from the data area to the buffer area at one stroke by inputting an address. *See* col. 21, lines 34-44.

CONCLUSION

4. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure.

Norman et al. **US Patent No. 6,175,937**

This patent discloses an apparatus and method for programming the memory cells of a multistate memory wherein the method involves the collapsing of data before transmitting to the memory cells, and a controller generates optimized program pulses of high voltage to apply to the memory cells, and wherein the pulses vary in amplitude and time, depending on the state level being transitioned, and wherein program verify is performed by reading the programmed data back into the controller where it is compared with the original value intended for programming.

This compare operation modifies the data read and initial data to reflect which memory cells require further programming, and the the modified data is again collapsed and sent to the memory for further programming and verify cycles until a monitoring circuit within the controller detects that no further programming is required

Sato et al. **US Patent No. 6,385,085**

This patent discloses a nonvolatile semiconductor memory in which multiple-value information is stored in one memory cell by setting a plurality of threshold values, data is successively read from word lines while continuously changing the word-line read level from a lowest level to a highest level, and the next bit line is selectively precharged in accordance with the data stored in latch means for storing read data.

Yamagami et al. **US Patent No. 5,644,539**

This patent discloses a semiconductor disk wherein a flash memory into which data is rewritten in block unit is employed as a storage medium, said semiconductor disk comprises a data memory in which file data are stored, a substitutive memory which substitutes for blocks of errors in the data memory, an error memory in which error information of the data memory are stored, and a memory controller which reads data out of, writes data into and erases data from the data memory, the substitutive memory and the error memory. Since the write errors of the flash memory can be remedied, the service life of the semiconductor disk can be increased.

Roohparvar **US Patent No. 5,615,159**

This patent discloses a memory system (preferably implemented as an integrated circuit) including an array of memory cells, a control unit for controlling operations of the system (such as programming, reading, and erasing the cells), at least one data storage unit which stores control parameter data determining at least one control parameter for the system, and default parameter circuitry for asserting at desired times one or both of: default control parameter data (regardless of the control parameter data stored in each data storage unit); and at least one default voltage level (in place of an otherwise asserted voltage level). In preferred embodiments, the default control parameter data (or voltage levels) are asserted during a test initialize mode in response to an initialization signal generated by the control unit, for use in initializing internal control registers (and voltage levels) of the system so that an external program for controlling the system during the test mode can start from a known condition. Other embodiments are methods for asserting default control parameter data of memory systems at desired times during systemoperation (regardless of the values of control parameter data stored in storage units of the system), methods for asserting default voltage values at desired times during operation of such systems, and memory systems capable of performing such methods.

Sasaki et al. **US Patent No. 5,469,390**

This patent discloses a semiconductor memory system including a plurality of memory chips, a spare memory is shared among the memory chips, and wherein a common redundant circuit and an external terminal capable of accessing to a spare memory are added to a semiconductor memory system, and a first region for storing a defect address in each memory of the

semiconductor memory system and a second region for storing a defect address of the system of the object having the same structure as the first region are provided in the redundant circuit, and . when the defect of a normal memory of the semiconductor memory system can not be replaced with the spare memory of the system itself, replacement is made possible with other system having the same structure, such that the yield of the semiconductor memory system can be increased, and the reliability is also increased.

Tobita et al. **US Patent No. 5,530,673**

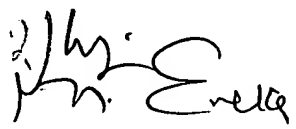
This patent discloses control method and system wherein a flash memory is used as a semiconductor disk or a main memory in an information processing system, and a semiconductor file system comprising a first nonvolatile memory electrically erasable, a second nonvolatile memory not electrically erasable, a volatile memory, a controller which controls the memories, and a control section which controls the controller wherein a physical address corresponding to a logical address specified from an external system is accessed, and wherein the first nonvolatile memory stores data for the external system to perform operations, first management information indicating the correspondence between physical addresses at which the data is stored and logical addresses, and second management information indicating a state of the first nonvolatile memory, the second nonvolatile memory previously stores interface information required for inputting and outputting the data from and to the external system and read-only data of the data, and the controller comprises control means for determining a physical sector address forming predetermined high-order bits of the physical address when data is output from the first nonvolatile memory or when data is input to the volatile memory, means for storing the

determined physical sector address, and means for consecutively generating addresses in a sector determined by the physical sector address.

4.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emeka J. Amanze, JD whose telephone number is (703) 305 0080. The examiner can normally be reached on Monday-Friday 8:30 am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady, can be reached at (703) 305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-9000.



Emeka J. Amanze, JD
Patent Examiner
Art Unit 2133

06/05/2002